

Amendments to the Claim:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 - 7 (canceled)

Claim 8 (previously presented): A microprocessor for processing various assembler codes, comprising:

a multiplexer having a first input, a second input for receiving a 0 value, and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place;

a program counter;

a computation unit for computing relative addresses;

an adding unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit;

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a subtracting unit connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit; and

a memory for storing an instruction length and having an output connected to said first input of said multiplexer.

Claim 9 (new): A microprocessor for processing various assembler codes, comprising:

a multiplexer having a first input, a second input for receiving a 0 value; and a third input receiving a parameter designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place;

a program counter;

a computation unit for computing relative addresses;

a memory for storing an instruction length and having an output connected to said first input of said multiplexer;

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and

an adding unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit; or

a subtracting unit connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit

~~a memory for storing an instruction length and having an output connected to said first input of said multiplexer.~~

Claim 10 (new): A microprocessor for processing various assembler codes, comprising:

a multiplexer having a first input, a second input for receiving a 0 value, and a third input receiving a parameter

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designating a respective assembler code and, depending on how the parameter is set, a different relative addressing takes place;

a program counter;

a computation unit for computing relative addresses;

a memory for storing an instruction length and having an output connected to said first input of said multiplexer;

an adding unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit;

a subtracting unit connected between said program counter and said computation unit for the relative addresses, said subtracting unit having a first input connected to said program counter, a second input connected to said multiplexer, a third input receiving the parameter and an output connected to said computation unit; and

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said adding unit and said subtracting unit being a combined
unit.